ELECTRONIC DEVICES AND AMPLIFIER CIRCUITS LAB

Subject Code: 20EC3351

Department of Electronics & Communications Engineering

PREPARED BY
DEPT OF ECE
Prasad V. Potluri Siddhartha Institute of Technology

ELECTRONIC DEVICES AND AMPLIFIER CIRCUITS LAB

Course Code	**20EC3351**	**Year**	II	**Semester**	I
Course Category	Program Core	**Branch**	ECE	**Course Type**	Lab
Credits	1.5	**L-T-P**	0-0-3	**Prerequisites**	Nil
Continuous Internal Evaluation	15	**Semester End Evaluation**	35	**Total Marks**	50

Course Outcomes	
Upon successful completion of the course, the student will be able to	
CO1	**Analyze** the devices BJT and MOSFET to model their small signal behavior. (L4)
CO2	**Apply** the network analysis techniques to find the parameters of BJT and MOSFET based amplifiers. (L3)
CO3	**Analyze** NMOS differential amplifiers for gain, input common mode range, power dissipation and CMRR. (L4)
CO4	**Evaluate** the performance of NMOS Current Mirror and to develop PCB Layout for Astable Multivibrator.(L5)
CO5	Make an effective report based on experiments

Contribution of Course Outcomes towards achievement of Program Outcomes & Strength of correlations (3:High, 2: Medium, 1:Low)

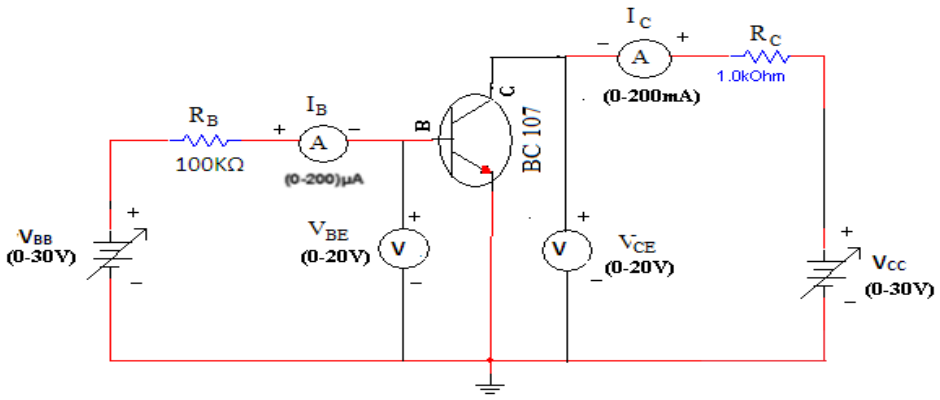
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO11	PO12	PSO1	PSO2
CO1		3							3				3	
CO2	3								3				3	
CO3		2							2				2	
CO4			2						2				2	
CO5										3				
Average* (Rounded to nearest integer)	3	3	2						3	3			3	

Syllabus

Any Ten Experiments (H/W or Simulation)		
Expt. No.	**Contents**	**Mapped CO**
1	Voltage-Current Characteristics of BJT / Measurement of scale current & common emitter current gain	**CO1, CO5**
2	Measurement of small signal parameters (g_m, r_o, r_π, r_e) of BJT at a given operating (Q) point.	**CO1 CO5,**
3	Implement BJT amplifier and Inverter logic gate	**CO2, CO5**
4	Voltage-Current Characteristics of MOSFET / Measurement of threshold voltage	**CO1, CO5**
5	Measurement of small signal parameters (g_m, ro, g_{mb}) of MOSFET at a given operating point	**CO1, CO5**
6	Analyze Common Source Amplifier for Gain, Power dissipation requirements	**CO2, CO5**
7	Design and Simulation of Common Drain Amplifier (Voltage Buffer) for Gain, Output Impedance, Level Shift requirements	**CO2, CO5**
8	Analyze the necessary parameters for Basic NMOS Differential Pair	**CO3, CO5**
9	Design and Simulation of Differential Amplifier with active current mirror load for gain, power dissipation CMRR requirements.	**CO3, CO5**
10	Analyze the basic NMOS current mirror and current steering circuit	**CO4, CO5**
11	Simulate the PCB fabrication of a BJT Multivibrator Circuit	**CO4, CO5**

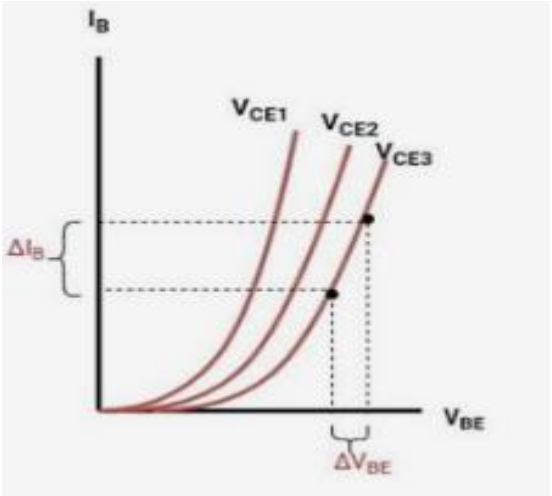
Learning Resources
Text Books
1. Adel S. Sedra, Kenneth C. Smith, Arun N. Chandorkar, Microelectronic Circuits, 6/e, Oxford University Press, 2013
Reference Books
1. Behzad Razavi, Fundamentals of Microelectronics, 2/e, Wiley Student Edition, 2013. 2. R.L.Boylestad, Louis Nashelsky, Electronic Devices and Circuits Theory, 10/e, Pearson, 2009. 3. Dharma Raj Cheruku, B T Krishna, Electronic Devices and Circuits, 2/e, Pearson, 2008.
e- Resources & other digital material
1. https://www.researchgate.net/publication/314154179_Electronics_Lab_Manual 2. http://abexp.aiaiai.dk/electronic_devices_and_circuits_lab_manual_bgpltd.pdf

Circuit Diagram:

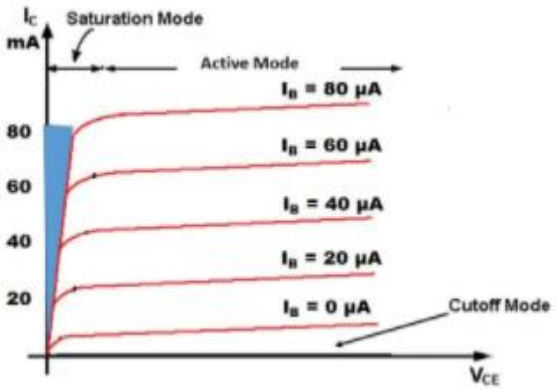


Model Graph:

Input characteristics



Output characteristics



Expt.No -1 **Date:**

VOLTAGE-CURRENT CHARACTERISTICS OF BJT / MEASUREMENT OF SCALE CURRENT & COMMON EMITTER CURRENT GAIN

Aim: To plot the input & output characteristics of an NPN transistor in common emitter configuration and to measure the scale current and common emitter current gain (β).

Components & Equipment Required:

S.No	Apparatus	Specifications	Quantity
1	Transistor	BC-107	1
2	Regulated power supply	0-30V	2
3	Voltmeter	0-20V	2
4	Ammeters	0-200mA 0-200μA	1 1
5	Resistors	100k Ω 470Ω	1 1
6	Bread board and connecting wires	----	-----

Theory: Transistor can be connected in a circuit in any of the three different configuration namely common base, common collector, common emitter. The common emitter mode is most used configuration as it provides voltage, current and power gains more than unity.

In CE configuration, the emitter of the transistor is common to the input and output circuits. Input signal is applied across the base and emitter and the output is taken across the collector and emitter. CE configuration is also grounded emitter configuration.

Dynamic input resistance (R_i):

The dynamic input resistance can be calculated from the input characteristic curves. It is given by the ratio of small change in collector to emitter voltage to corresponding change in base current, keeping collector to emitter voltage constant.

$$R_i = \Delta V_{BE} / \Delta I_B \mid V_{CE} \text{ constant}$$

Observations:

Input characteristics:

S.NO	V_{BB}(V)	V_{CE} = 1V		V_{CE} = 2V	
		V_{BE}(V)	I_B(μA)	V_{BE}(V)	I_B(μA)

Dynamic output resistance (R_O):

The dynamic output resistance can be calculated from the output characteristic curves. It is given by the ration of small change in collector to emitter voltage to corresponding change in collector current, keeping base current constant.

$$R_O = \Delta V_{CE} / \Delta I_C \mid I_B \text{ constant}$$

Common emitter current gain (β):

The common current gain β is the ratio of change in collector current to the corresponding change in base current, keeping the collector to emitter voltage constant.

$$\beta = \Delta I_C / \Delta I_B \mid V_{CE} \text{ constant}$$

PROCEDURE:

INPUT CHARECTERSTICS:

1. Connect the circuit as per the circuit diagram.
2. For plotting the input characteristics the output voltage V_{CE} is kept constant at 1V by varying V_{CC}.
3. By varying V_{BB} note down the corresponding values of V_{BE} & I_B.
4. Repeat the above steps 2 & 3 for different values of V_{CE}.
5. Tabulate all the readings.
6. plot the graph between V_{BE} and I_B for constant V_{CE}
7. Calculate the dynamic input resistance R_i.

OUTPUT CHARACTERSTICS:

1. Connect the circuit as per the circuit diagram
2. For plotting the output characteristics the input current I_B is kept constant at 10μA by varying V_{BB}.
3. By varying V_{CC} note down the corresponding values of V_{CE} & I_C.
4. Repeat the above steps 2 & 3 for different values of I_B.
5. Tabulate the all the readings.
6. Plot the graph between V_{CE} and I_C for constant I_B
7. Calculate the common current gain β and Scale current I_S.

Output characteristics

S.NO	V_{CC}(V)	I_B = 10 μA		I_B = 20μA	
		V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_CmA)

Calculations:

Dynamic input resistance of transistor in CE configuration:

$$R_i = \Delta V_{BE} / \Delta I_B \mid V_{CE} \text{ constant}$$

$$\beta = I_C / I_B \mid V_{CE} \text{ constant}$$

Scale current: The current I_S is usually called as saturation current the other name for saturation current is called as scale current given by the formula

$$I_C = I_S \, e^{V_{BE} / V_T}$$

$$I_S = I_C / e^{V_{BE} / V_T}$$

Precautions:

1. The supply voltage should not exceed the rating of the transistor
2. Meters should be connected properly according to their polarities
3. If the ammeter does not show any deflection, the circuit may be open somewhere
4. Verify the connections using multi meter.

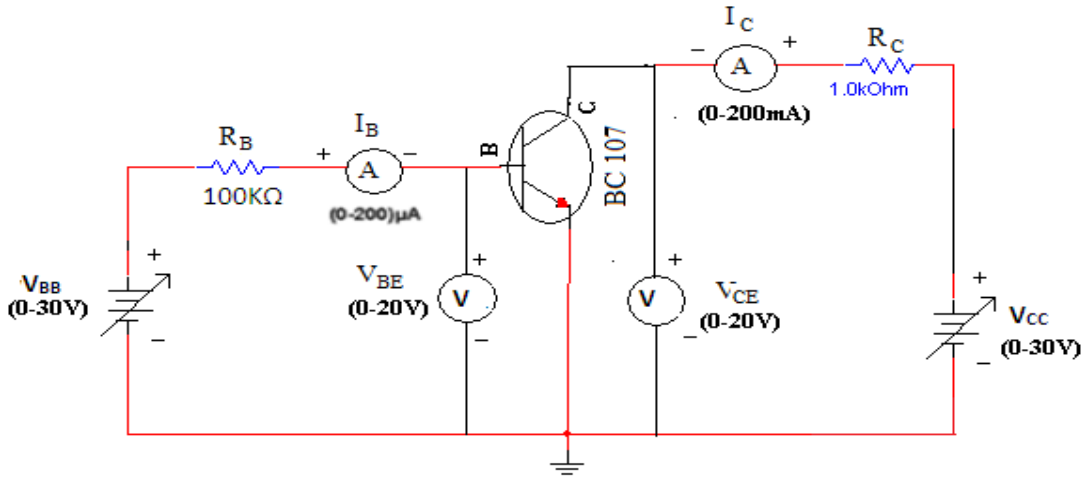
Result: Hence,

- The input & output characteristics of transistor in Common Emitter configuration has been plotted
- Calculated the Scale current I_S and common emitter current gain (β).

Viva-voce Questions:

1. What is β? Give its typical value.,
2. What is the importance of CE amplifier?
3. What is the significance of h_{FE}? How is it different from h_{fe}?
4. What is early effect
5. What is loading effect?

Circuit Diagram



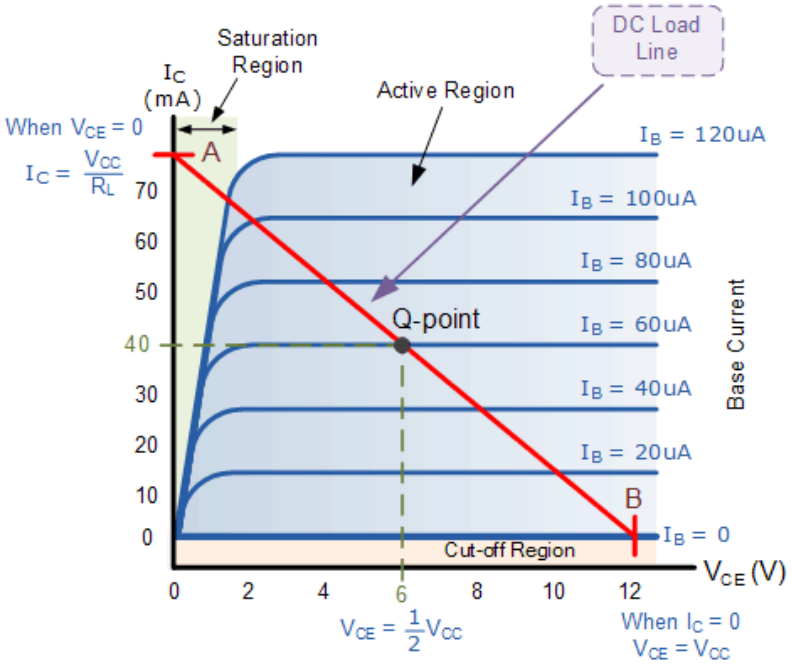
Calculations:

$V_{CC} = I_C R_C + V_{CE}$

$V_{CE(max)} = V_{CC}$ at $I_C = 0$

$I_{C(max)} = V_{CC}/R_C$ at $V_{CE} = 0$

Model Graph for Q-point:



Expt.No -2 **Date:**

Measurement of small signal parameters (g_m, r_o, r_π, r_e) of BJT at Operating (Q) Point

Aim:

To plot DC load line of a npn BJT, mark operating point Q and calculate small signal parameters/ h parameters **g_m, r_o, r_π and r_e** from I –V characteristics.

Apparatus:

S.No	Apparatus	Specifications	Quantity
1	Transistor	BC-107	1
2	Regulated power supply	0-30V	2
3	Voltmeter	0-20V	2
4	Ammeters	0-200mA 0-200µA	1 1
5	Resistors	100k Ω 470Ω	1 1
6	Bread board and connecting wires	----	-----

Theory:

Transistor can be connected in a circuit in any of the three different configuration namely common base, common collector, and common emitter. The common emitter mode is most commonly used configuration as it provides voltage, current and power gains more than unity. In CE configuration, the emitter of the transistor is common to the input and output circuits. Input signal is applied across the base and emitter and the output is taken across the collector and emitter. CE configuration is also grounded emitter configuration.

Consider a transistor operating in the active region at the point labelled Q in Fig below that is, at a collector current I_{CQ}, a base current I_{BQ}, and a collector-emitter voltage V_{CEQ}. The ratio of the collector current to the base current is the large-signal or dc β.

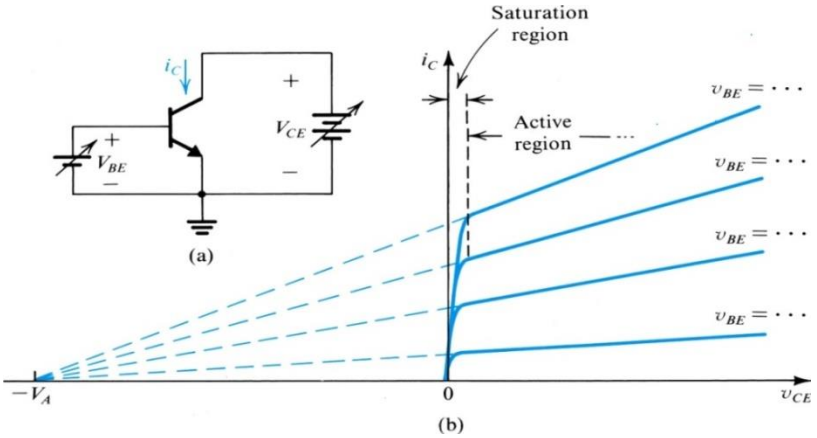
$$\beta_{dc} \equiv \frac{I_{CQ}}{I_{BQ}}$$

Dynamic input resistance (R_i):

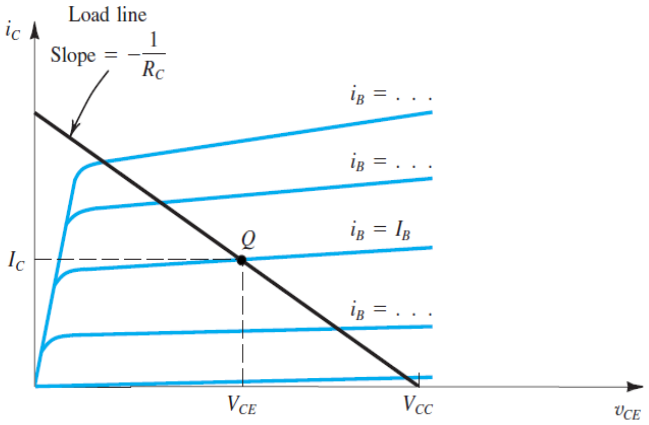
The dynamic input resistance can be calculated from the input characteristic curves. It is given by the ratio of small change in collector to emitter voltage to corresponding change in base current, keeping collector to emitter voltage constant.

$$R_i = \Delta V_{BE} / \Delta I_B \mid V_{CE} \text{ constant}$$

Finding V_A :



a) Draw the DC load line and obtain Q-point coordinates:



Observations:

Output Characteristics:

V_{CC} (V)	I_B = 10µA		I_B = 30µA	
	V_{CE}(V)	I_C (mA)	V_{CE}(V)	I_C (mA)
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				

Calculations:

$\beta =$

$I_{C\,max} =$

$V_{CEQ} =$

$I_{CQ} =$

$g_m = I_{CQ}/V_T =$

$r_\pi = \beta/g_m =$

$r_e = r_\pi / (1+\beta) =$

$r_o = \frac{V_A + V_{CEQ}}{I_{CQ}} =$

Procedure for Measurement of small signal parameters (g_m, r_o, r_π, r_e)

1. From the output characteristics, draw the DC load line and obtain Q-point coordinates
2. From I_{CQ}, V_{CEQ} values use the following formulas to calculate small signal parameters

$g_m = I_C / V_T$ $\quad r_e = V_T / I_E$ $\quad r_\pi = \beta / g_m$ $\quad r_o = \dfrac{V_A + V_{CEQ}}{I_{CQ}}$

where V_A is measured as shown in the above characteristics.

V_T =25mV at room temperature.

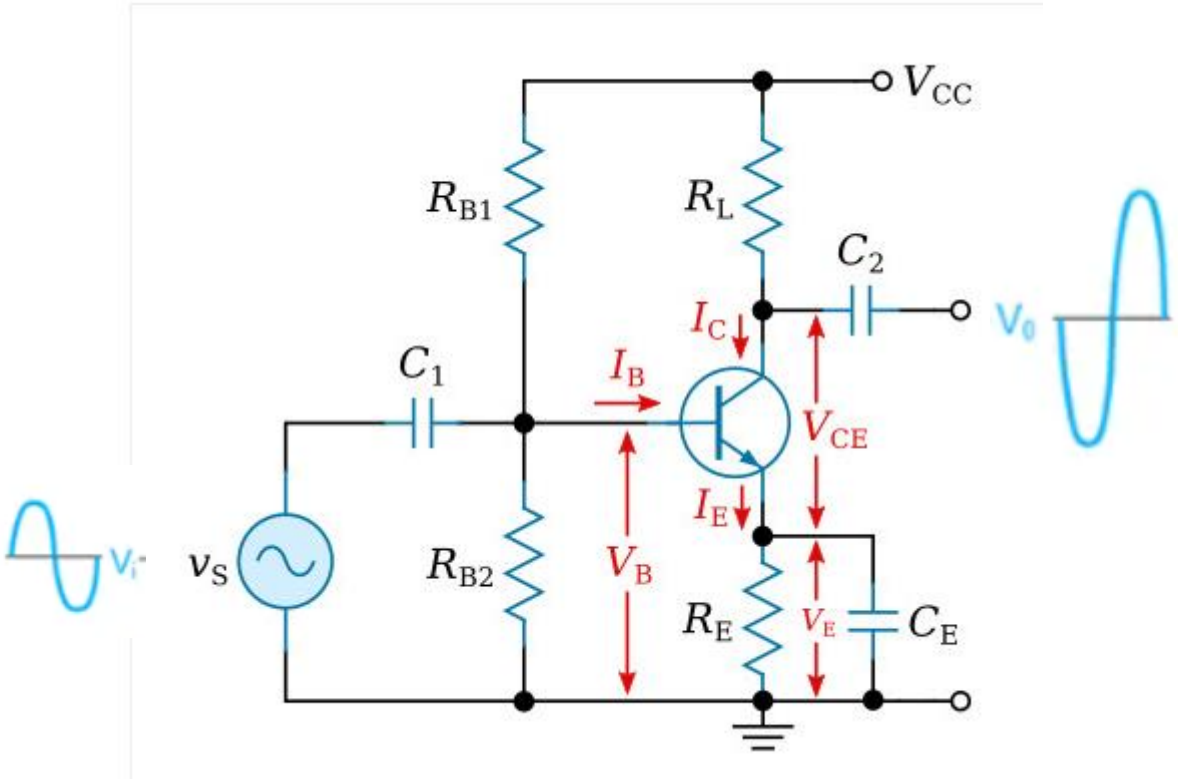
β=110. (This is not fixed. you have to measure by using multimeter.)

Precautions:

- If the ammeter does not show any deflection, the circuit may be open some where
- Verify the connections using multimeter.
- If the ammeter doesn't show any deflection further, verify the condition of the transistor and replace (if necessary).
- Reduce the value of the emitter base resistor if necessary for sufficient amount of base currents to be generated.

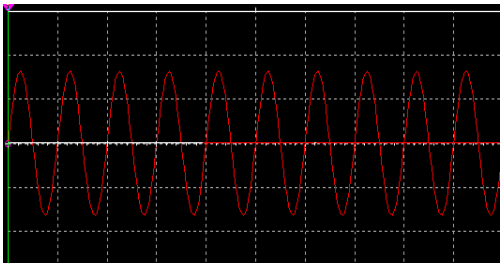
Result:

Circuit Diagram

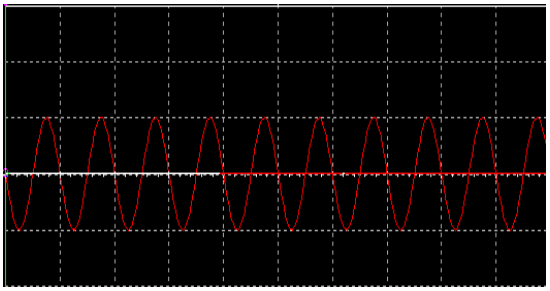


Model Graph for Q-point:

Input graph



Output graph



EXP-3 Date:

Implement BJT amplifier and Inverter logic gate

3.a) BJT AMPLIFIER (Common-Emitter Amplifier)

Aim: Implement BJT amplifier for the given specifications of V_{CC} =12V; I_C = 4.5mA; V_{BE} =0.7V

Apparatus:

S.No	Apparatus	Specifications	Quantity
1	Transistor	BC-107	1
2	Regulated power supply	0-30V	2
3	Voltmeter	0-20V	2
4	Function generator		
5	Resistors		1 1
6	Capacitors		
7	Bread board and connecting wires	----	-----

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DESIGN PROCEDURE:

V_{CC} is taken 20% more than the required output swing.

V_{CC} =12v; I_C =4.5mA; V_{BE} =0.7v

To make an operating point in the middle of the load line assume DC conditions.

$V_{RC} = 40\% of\ V_{CC} = 4.8V$

$VRE = 10\%\ of\ V_{CC} = 1.2V$

$V_{CE} = 50\%\ \ of\ V_{CC} = 6V$

To find $R_E : R_E = \frac{V_{RE}}{I_C} = \frac{1.2}{4.5mA} = 270\Omega$

To find R_C :

$V_{CC} - I_C R_C - V_{CE} - V_{RE} = 0$

$R_C = 1K\Omega$

To find R_1 & R_2 :

$V_B = V_{BE} + V_{RE}$

$V_B = 1.9V$

[When measured with millimetre β =236]

$I_C = \beta I_B$

$I_B = 19\mu A$

Assume $10I_B$ *flowsthrough* R_1 & I_B *flowsthrough* R_2 *then*

$R1 = \frac{V_{CC} - V_B}{10I_B} = 68K\Omega$

$R_2 = V_B / 9I_B = 14K\Omega$

To find C_E :

$f_l = 265Hz$

$f_l = \frac{1}{2\Pi R_E C_E};$

$C_E = 100\mu F$

To design Cc_1 :

$f_L = \frac{1}{2\Pi(\frac{R_i}{10})Cc1}$; $R_I = R_1 \| R_2 \| h_{ie;}$

$C_{C1} = 3.8\mu F$

To design Cc_2 :

$Cc_2 = \frac{1}{2\Pi(\frac{R_0 + R_2}{10}) f_2}$

$Cc_2 = 3\mu F$

OBSERVATIONS:

Gain $= \frac{V_O}{V_I};$

PROCEDURE:

1. Connect the circuit diagram as shown in Figure.
2. Keep VS at 5 mv, using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0 to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph taking time period on the x-axis and amplitude on the y-axis.

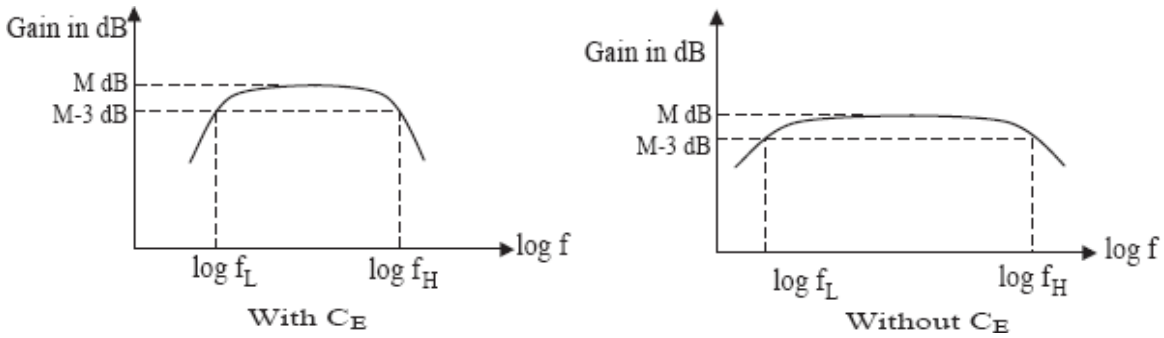
OBSERVATIONS:

From CRO:

1. Input voltage V_i =
2. Output voltage V_0 =
3. Voltage gain $A_V=V_0/V_i$=

S.NO	Frequency(Hz)	Vo(volts)	Gain Av = vo/vs	Gain in dB = 20logAv

Graph:



RESULT:

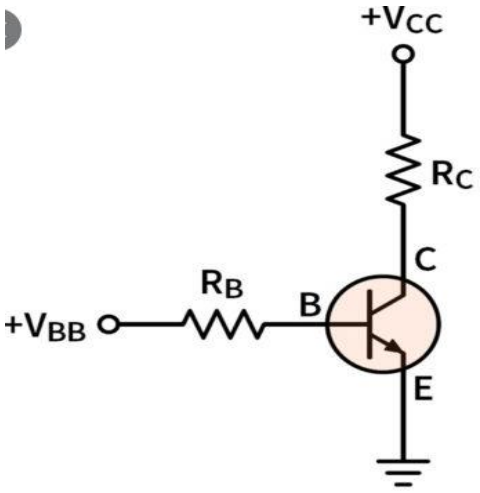
3.b)BJT as an inverter logic gate

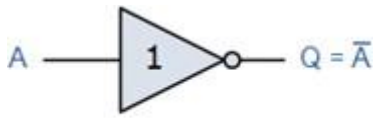
AIM: Simulate and Implement BJT as an Inverter logic gate by using MULTISIM software

EQUIPMENT REQUIRED FOR HARDWARE:

R.P.S (0-30V), C.R.O, Transistor (BC107), Function generator, Resistors

CIRCUIT DIAGRAM:





Inverter or NOT Gate

PROCEDURE:

1. Connect the circuit diagram as shown in Figure.
2. Apply 0 V and 5V observe the output in the multimeter.
3. Plot the graph taking input voltage on the x-axis and output voltage on the y-axis.

TABULAR FORM:

S.NO	**V_i**	**V_o**

RESULT:

EXP-4 Date:

Voltage-Current Characteristics of MOSFET / Measurement of threshold Voltage

AIM: To plot the Transfer and Drain characteristics of MOSFET and determine threshold voltage.

APPARATUS:

S.No	Name	Range/Value	Quantity
1	Dual Channel DC RPS	(0-30)V	1
2	Transistor(MOSFET)	2N7000	1
3	D.C Ammeters	0-200μA)	Each 1
4	D.C Volt meters	(0-20)V	1
5	Bread Board and connecting wires		1 Set

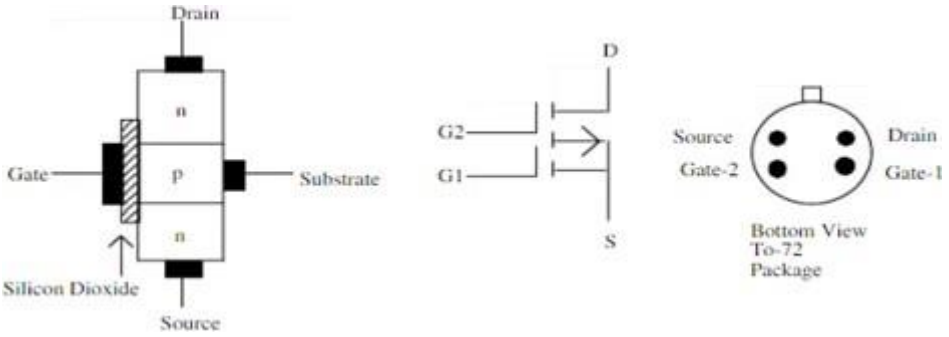
THEORY:

The MOSFET is actually a four-terminal device, whose substrate, or body terminal must be always held at one of the extreme voltage in the circuit, either the most positive for the PMOS or the most negative for the NMOS. One unique property of the MOSFET is that the gate draws no measurable current. MOSFET is a voltage controlled device. It has very high input impedance and works at high switching frequency.

MOSFET's are of two types 1) Enhancement type 2) Depletion type.

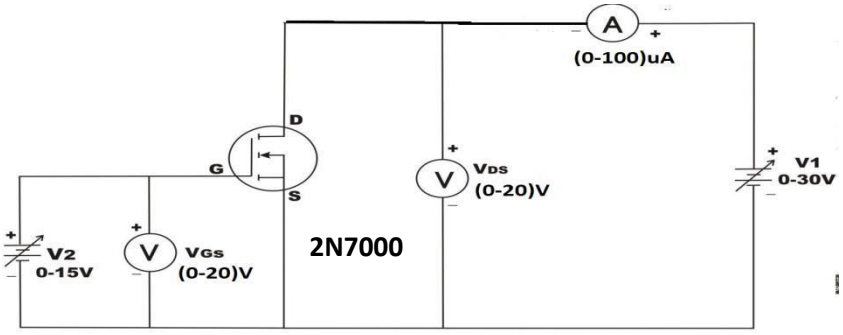
A metal oxide semiconductor field effect transistor (MOSFET) is a semiconductor device similar to junction field effect transistor (JFET). JFET is the result of the search for high input resistance transistor and MOSFET is result of bipolar gate bias.. The major structural design change between the JFET and the MOSFET is insulating SiO_2 layer between the gate and the conducting channel. This insulating layer gives very high input resistance to the device. There is no electrical connection between the gate and the conducting channel. The electric field controls the device current. The current flow between the source and drain terminals is controlled by gate source voltage V_{GS} applied between the gate and source. If the gate source voltage is below a threshold voltage V_t the MOSFET does not conduct or the device is off. When V_{GS} is greater than the threshold voltage then drain current flows. The threshold voltage is positive for n-channel MOSFET and itis negative for p-channel

MOSFET. All the equations of JFET hold good for MOSFET with pinch-off voltage replaced by threshold voltage in MOSFET



A negative gate potential results in depletion mode of operation and positive gate potential results in enhancement mode of operation. The value of at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the threshold voltage and is denoted V_t

CIRCUIT DIAGRAM:



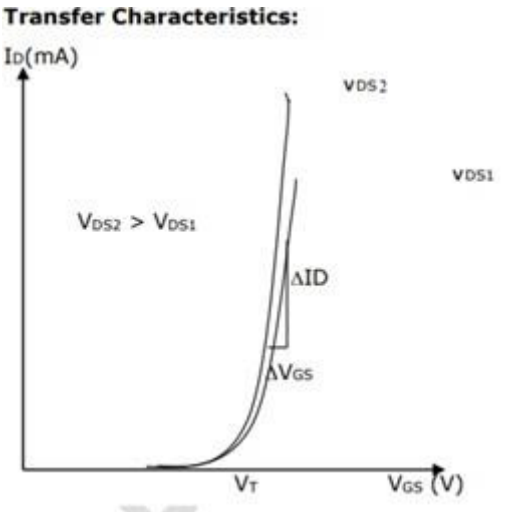
PROCEDURE:

A) TRANSFER CHARACTERISTICS:

1. Make the connections as per the circuit diagram.
2. Initially keep V_{GG} and V_{DD} at 0 V.
3. Switch ON the regulated power supplies. Set the voltage VDS constant at 5V and 10 V.
4. Vary V_{GG} in steps of 0.5V upto 5V and at each step note down the correspondingvalues of V_{GS} and I_D. (Note: note down the value of V_{GS} at which I_D startsincreasing as the threshold voltage).
5. Reduce V_{GG} and V_{DD} at 0 V.
6. Repeat step 3 and 4.
8. Plot a graph of V_{GS} versus I_D for different values of V_{DS}.

TRANSFER CHARACTERISTICS:

V_{GG}(V)	VDS1= 1Volts		VDS2= 2Volts	
	VGS (V)	ID (mA)	VGS (V)	ID (mA)
0				
0.1				
0.2				
0.3				
0.4				
0.5				
0.6				
0.7				
0.8				
0.9				
1				



B) DRAIN CHARACTERISTICS OR OUTPUT CHARACTERISTICS:

1. Make the connections as per the circuit diagram.
2. Initially keep V_{GG} and V_{DD} at 0 V
3. By varying V_{GG}, set V_{GS} to some constant voltage (must be more than Threshold voltage).
4. By gradually increasing V_{DD}, note down the corresponding value of V_{DS} and I_D.
5. (Note: Till the MOSFET jumps to conducting state, the voltmeter which is connected across device as V_{DS} reads approximately zero voltage. Further increase in voltage by V_{DD} source cannot be read by V_{DS}, so connect millimeter to measure the voltage.)
6. Set V_{GS} to some other value (more than threshold voltage) and repeat step 4.
7. Plot a graph of V_{DS} versus I_D for different values of V_{GS}.

Note: If V_{DS} is lower than V_P (pinch-off voltage) the device works in the constant resistance region that is linear region. If V_{DS} is more than V_P, a constant ID flows from the device and this operating region is called constant current region

Threshold voltage V_T : Gate to source voltage at which, drain current starts flowing.

$$V_{th} = V_{T0} + \gamma(\sqrt{|2\phi_F - V_{SB}|} - \sqrt{|2\phi_F|})$$

γ -Body –Effect Parameter is $0.4V^{1/2}$

V_{SB}=source to bulk voltage. (Reverse Bias Voltage between source and body)

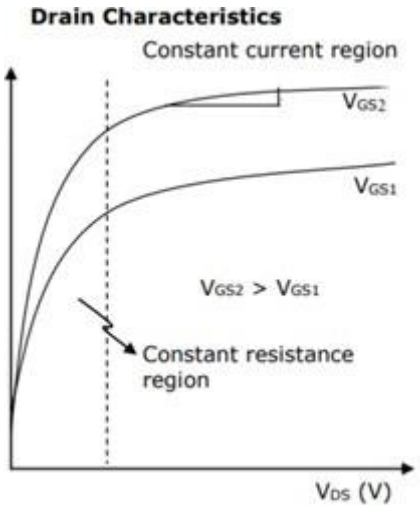
V_{T0}= the threshold voltage with VSB =0 i.e. with out the body effect.

ϕ_F-Physical Parameter with $2\phi_F$=0.6 V for NMOS

DRAIN CHARACTERISTICS

V_{DD}(V)	VGS1= 0.5 Volts		VGS2= 1 Volts	
	VDS (V)	ID (mA)	VDS (V)	ID (mA)
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				

MODEL GRAPHS:



RESULT:

EXP-5 Date:

Measurement of small signal parameters (g_m, r_o, g_{mb}) of MOSFET at a given operating point.

AIM: From the I-V characteristics of a MOSFET with a given Q-point ,measure small signal parameters g_m, r_o, g_{mb}

APPARATUS:

Sl.No	Name	Range/Value	Quantity
1	Dual Channel DC RPS	(0-30)V	1
2	Transistor(MOSFET)	2N7000	1
3	D.C Ammeters	0-200μA)	Each 1
4	D.C Volt meters	(0-20)V	1
5	Bread Board and connecting wires		1 Set

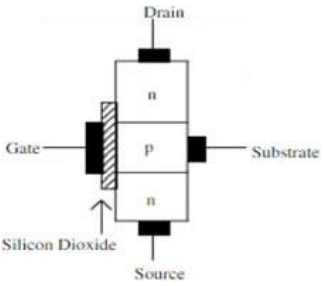
THEORY:

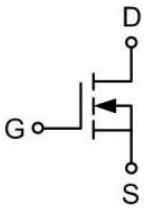
The MOSFET is actually a four-terminal device, whose substrate, or body terminal must be always held at one of the extreme voltage in the circuit, either the most positive for the PMOS or the most negative for the NMOS. One unique property of the MOSFET is that the gate draws no measurable current. MOSFET is a voltage controlled device. It has very high input impedance and works at high switching frequency.

MOSFET's are of two types 1) Enhancement type 2) Depletion type.

A metal oxide semiconductor field effect transistor (MOSFET) is a semiconductor device similar to junction field effect transistor (JFET). JFET is the result of the search for high input resistance transistor and MOSFET is result of bipolar gate bias.. The major structural design change between the JFET and the MOSFET is insulating SiO2 layer between the gate and the conducting channel. This insulating layer gives very high input resistance to the device. There is no electrical connection between the gate and the conducting channel. The electric field controls the device current. The current flow between the source and drain terminals is controlled by gate source voltage VGS applied between the gate and source. If the gate source voltage is below a threshold voltage Vt the MOSFET does not conduct or the device is off. When VGS is greater than the threshold

voltage then drain current flows. The threshold voltage is positive for n-channel MOSFET and itis negative for p-channel MOSFET. All the equations of JFET hold good for MOSFET with pinch-off voltage replaced by threshold voltage in

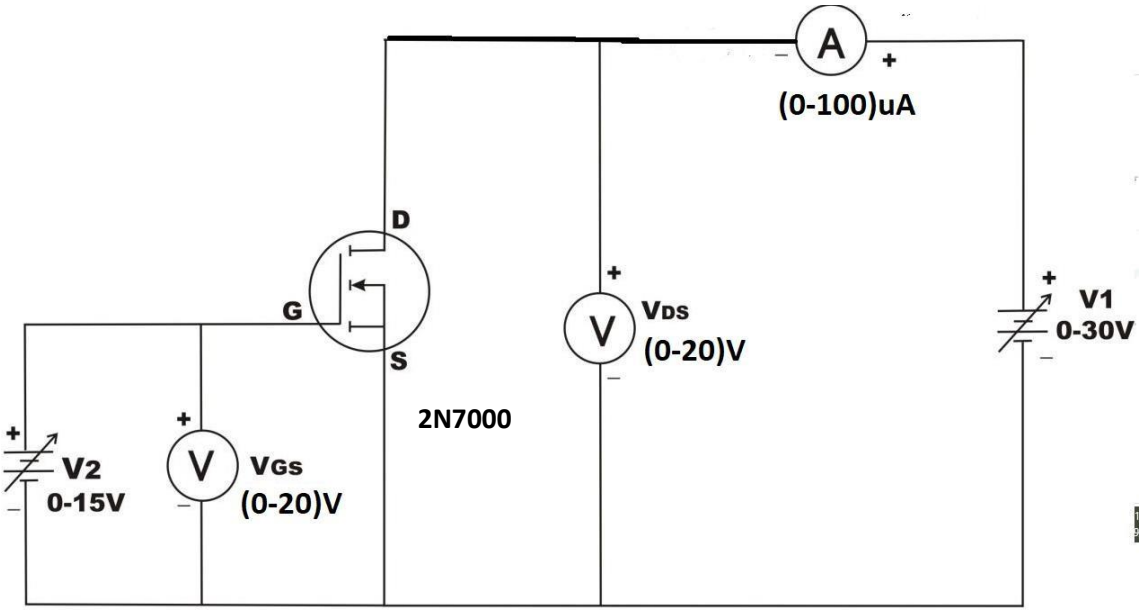




MOSFET

A negative gate potential results in depletion mode of operation and positive gate potential results in enhancement mode of operation. The value of at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the threshold voltage and is denoted Vt.

CIRCUIT DIAGRAM:



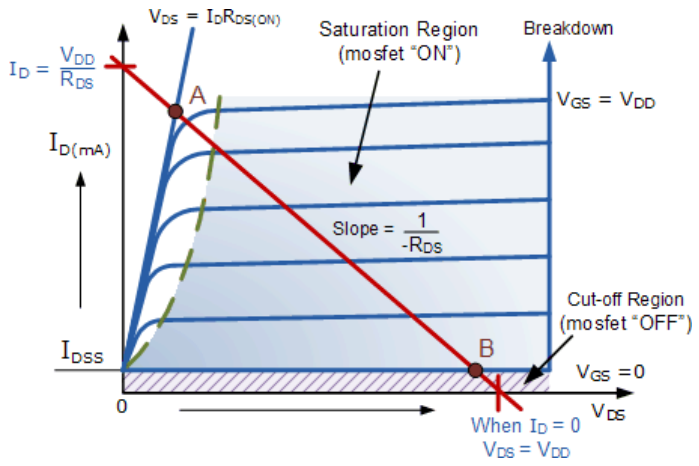
TABULAR FORM:

A) DRAIN CHARACTERISTICS:

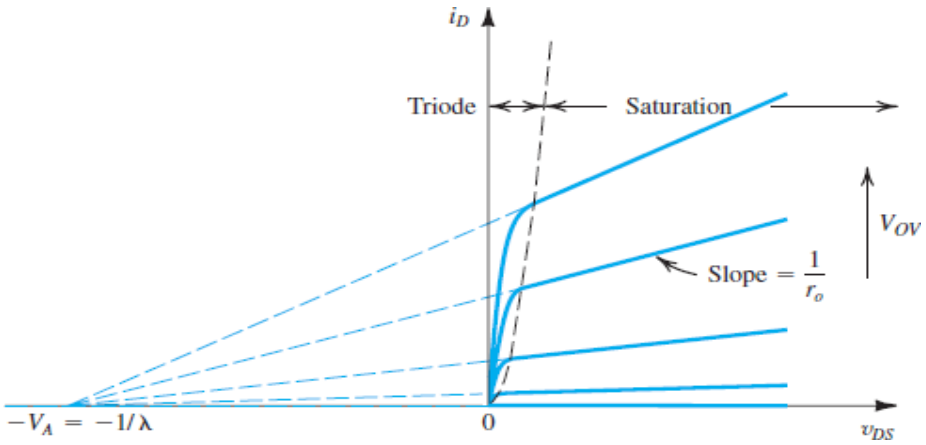
V_{DD}(V)	V_{GS1}= 1 Volts		V_{GS2}= 2 Volts	
	V_{DS} (V)	I_D (mA)	V_{DS} (V)	I_D (mA)
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				

Model Graphs:

A) DRAIN CHARACTERISTICS:



B) TO FIND EARLY VOLTAGE V_A :



PROCEDURE:

A. DRAIN CHARACTERISTICS:

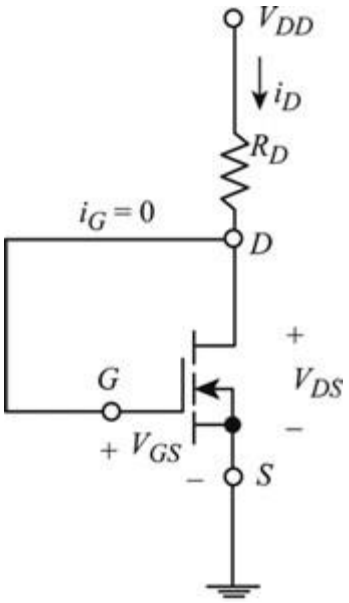
1. Make the connections as per the circuit diagram.
2. Initially keep V_{GG} and V_{DD} at 0 V
3. By varying V_{GG}, set V_{GS} to some constant voltage (must be more than Threshold voltage).
4. By gradually increasing V_{DD}, note down the corresponding value of V_{DS} and I_D. (Note: Till the MOSFET jumps to conducting state, the voltmeter which is connected across device as V_{DS} reads approximately zero voltage. Further increase in voltage by V_{DD} source cannot be read by V_{DS}, so connect millimeter to measure the voltage.)
5. Set V_{GS} to some other value (more than threshold voltage) and repeat step 4.
6. Plot a graph of V_{DS} versus I_D for different values of V_{GS}.

Note: If V_{DS} is lower than V_P (pinch-off voltage) the device works in the constant resistance region thatis linear region. If V_{DS} is more than V_P, a constant I_D flows from the device and this operating region iscalled constant current region.

CALCULATIONS:

1. Determine the Q point for the MOSFET in the circuit:

   The below figure represents the DC equivalent circuit of enhancement N–MOSFET.



A popular biasing arrangement for enhancement-type MOSFETs is provided. The resistor R_G brings a suitably large voltage to the gate to drive the MOSFET"on." Since I_G =0 mA and V_{RG} =0 V.
A direct connection now exists between drain and gate, resulting in

$$V_D=V_G \quad \text{and} \quad V_{DS}=V_{GS}=V_G-V_S$$

For the output circuit,

$$V_{GS}= V_{DS} = V_{DD} - I_D R_D$$

Here $V_{DS}= V_D - V_S$

$$V_{DD}=I_D R_D + V_{GS}$$

The V_{DD} is termed as DC load line equation.

To find the DC operating point of voltage, it is considered to be $I_D = 0$

$$V_{GSQ} = V_{DD} I_D = 0 \text{ mA}$$

To find the DC operating point of current, it is considered to be $V_{DS} = 0$,R_D=2KΩ

$$V_{DD} = I_{DQ} R_D$$

$$I_{DQ} \frac{V}{R_D} -$$

2. Small-Signal Parameters:

a) Transconductance :

$$g_m = k_n' \frac{W}{L} V_{OV} = \frac{2I_D}{V_{GS} - V_t} = \frac{2I_D}{V_{OV}}$$

b) Output Resistance :

$$r_o = \frac{VA}{I_D} = \frac{1}{I_D}$$

c) Body Transconductance:

$$g_{mb} = \frac{\gamma}{2\sqrt{2\emptyset_f + 7_{SB}}} g_m$$

γ - Body –Effect Parameter is 0.4 $V^{1}/_{2}$

V_{SB}=source to bulk voltage. (Reverse Bias Voltage between source and body)

V_{T0}= the threshold voltage with V_{SB} =0 i.e. with out the body effect.

ϕ_F-Physical Parameter with $2\phi_F$ = 0.6 V for NMOS

RESULT:

EXP-6 Date:

Analyze Common Source Amplifier for Gain, Power dissipation requirements

AIM: To obtain the frequency response of MOSFET amplifier in common source configuration with given specifications.

APPARATUS:

Resistors:100kΩ, 2.7kΩ, 470Ω,33kΩ,820kΩ.
Capacitors:1μF,10μF.
Regulated power supply
C.R.O
Function generator.

THEORY:

The MOSFET structure has become the most important device structure in the electronics industry. It dominates the integrated circuit technology in Very Large Scale Integrated (VLSI) digital circuits based on n-channel MOSFETs and Complementary nchannel and p-channel MOSFETs (CMOS). The technical importance of the MOSFET results from its low power consumption, simple geometry, and small size, resulting in very high packing densities and compatibility with VLSI manufacturing technology. Two of the most popular configurations of small-signal MOSFET amplifiers are the common source and common drain configurations. The common source circuit is shown below. The common sources, like all MOSFET amplifiers, have the characteristic of high input impedance. High input impedance is desirable to keep the amplifier from loading the signal source. This high input impedance is controlled by the bias resistors R1 and R2). Normally the value of the bias resistors is chosen as high as possible. However, too big a value can cause a significant voltage drop due to the gate leakage current. A large voltage drop is undesirable because it can disturb the bias point. For amplifier operation the MOSFET should be biased in the active region of the characteristics

CIRCUIT DIAGRAM:

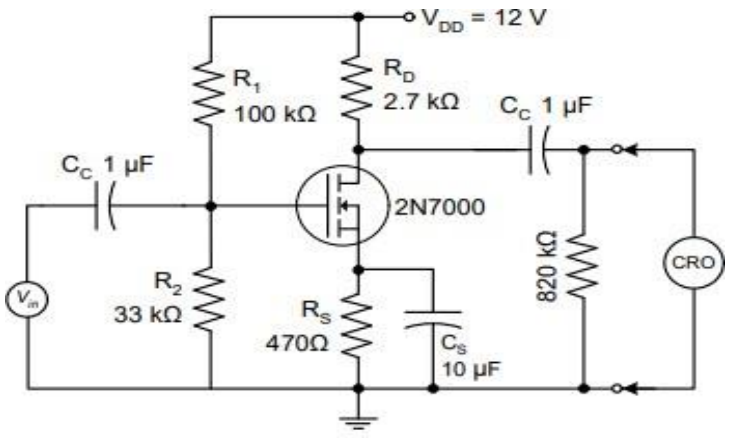


Fig. 1 Circuit diagram of MOSFET amplifier

DESIGN:

Assume V_{DD} = 12V, V_{RD} = 5V, V_{DS} = 6V, I_D = 2 mA

$$R_D = \frac{V_{RD}}{I_D} = \frac{5}{2\times10\times10^{-3}} = 2.5\ \text{k}\Omega \qquad \text{use 2.7 k}\Omega\text{ resistor.}$$

Now, the voltage across source side resistance $V_{RS} = V_{DD} - V_{DS} - V_{RD} = 12 - 6 - 5 = 1\ \text{V}$

As, $I_S = I_D$, (no current flows through the gate),

$$R_S = \frac{V_{RS}}{I_D} = \frac{1}{2\times10\times10^{-3}} = 500\ \Omega \qquad \text{use 470 }\Omega\text{ resistor.}$$

Voltage – divider bias circuit design:

Assume, R_1 = 100 kΩ. By, voltage division rule, R_2 can be obtained as,

$$V_G = V_{DD} \times \frac{R_2}{R_1 + R_2}$$

Selecting the value of V_G as 4V

$$4 = 12 \times \frac{R_2}{100\times10\times10^3 + R_2} \qquad R_2 \approx 47\ \text{k}\Omega$$

Design of capacitors:

Assume impedance of coupling capacitor be < 1.5 kΩ. Therefore,

$$X_{C1} \le 1.5\text{k}\Omega \qquad \text{ie} \quad \frac{1}{2\pi f C_1} \le 1.5\ \text{k}\Omega$$

Given, the frequency of the input signal is 100Hz.

C_1 = 1.06μf. use 1 μf capacitor.

Let $C_1 = C_2$ = 1 μf.

For the bypass capacitor,

$$X_{CS} \le 150\Omega \qquad \text{ie} \quad \frac{1}{2\pi f C_S} \le 150\ \Omega$$

C_S = 10μf

PROCEDURE:

Set up the circuit as shown in the figure with an input signal of 0.2V (peak-to-peak) at 1000 Hz. Observe the output on the CRO. Vary the frequency of the input signal over a range of values (from 50Hz to a few MHz) to obtain the frequency response which is a graph between log f (x-axis) and gain in dB (y-axis).

OBSERVATION:

Frequency f Hz	Input voltage V_i V	Output voltage V_i V	Gain $\frac{V_o}{V_i}$ -	Gain $20\log\frac{V_o}{V_i}$ dB

GRAPH (to be obtained):

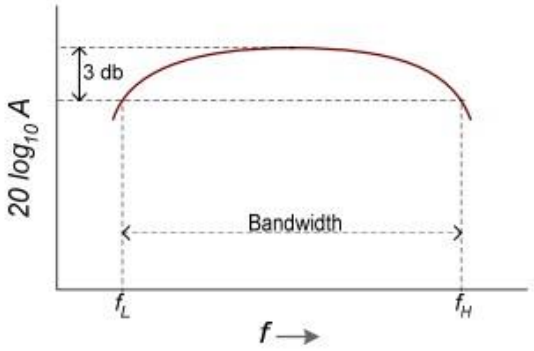


Fig 2. Frequency response

RESULT:

The required common source MOSFET amplifier was designed and set up to obtain the required frequency response.

EXP-7 Date:

Design and Simulation of Common Drain Amplifier (Voltage Buffer) for Gain, Output Impedance, Level Shift requirements

AIM: To Design and Simulate the Common Drain Amplifier (Voltage Buffer) .

a) Obtain the Gain and Output Impedance

b) Obtain the Level Shift requirements.

Experimental Requirements:

Resistors : 5MΩ , 40KΩ,10KΩ
Capacitors:0.1µF
Function generator.
C.R.O.
Regulated power supply.

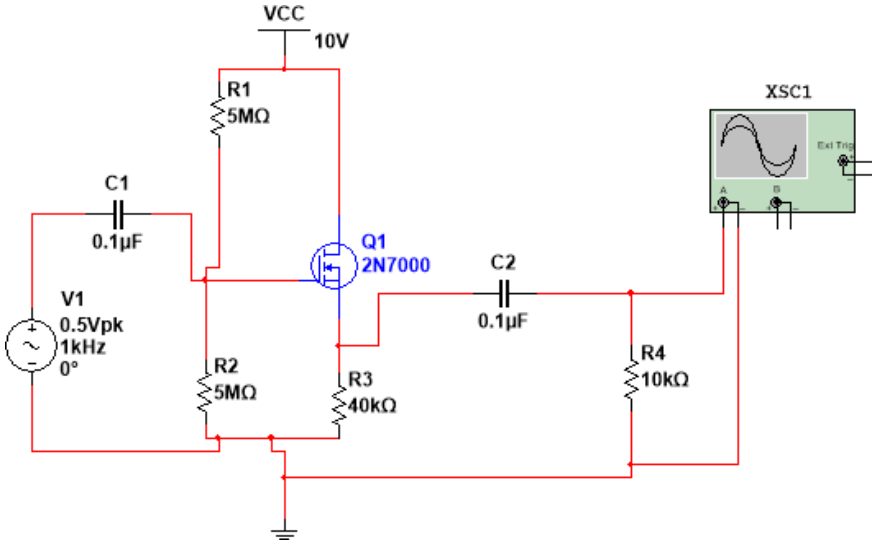
Theory :

The common-drain (CD) amplifier is comparable to the common-collector BJT amplifier. Recall that the CC amplifier is called an emitter-follower. Similarly, the common-drain amplifier is called a source-follower because the voltage at the source is approximately the same amplitude as the input (gate) voltage and is in phase with it. In other words, the source voltage follows the gate input voltage.

A common-drain amplifier is one in which the input signal is applied to the gate and the output is taken from the source, making the drain common to both. Because it is common, there is no need for a drain resistor. A common-drain amplifier is shown below. A common-drain amplifier is also called a source-follower. Self-biasing is used in this particular circuit. The input signal is applied to the gate through a coupling capacitor, and the output signal is coupled to the load resistor through the other capacitor.

	Definition	Expression	Approximate expression	Conditions
Current gain	$A_\mathrm{i} = \frac{i_\mathrm{out}}{i_\mathrm{in}}$	∞	∞	
Voltage gain	$A_\mathrm{v} = \frac{v_\mathrm{out}}{v_\mathrm{in}}$	$\frac{g_m R_\mathrm{S}}{g_m R_\mathrm{S} + 1}$	≈ 1	$(g_m R_\mathrm{S} \gg 1)$
Input impedance	$r_\mathrm{in} = \frac{v_{in}}{i_{in}}$	∞	∞	
Output impedance	$r_\mathrm{out} = \frac{v_{out}}{i_{out}}$	$R_\mathrm{S} \Vert \frac{1}{g_m} = \frac{R_\mathrm{S}}{g_m R_\mathrm{S} + 1}$	$\approx \frac{1}{g_m}$	$(g_m R_S \gg 1)$

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the circuit diagram as shown in Figure.
2. Keep Vin at 10 mv, using the function generator.
3. Keeping the input voltage constant, vary the frequency from 0 to 1 MHz in regular steps and note down the corresponding output voltage.
4. Plot the graph taking time period on the x-axis and amplitude on the y-axis.

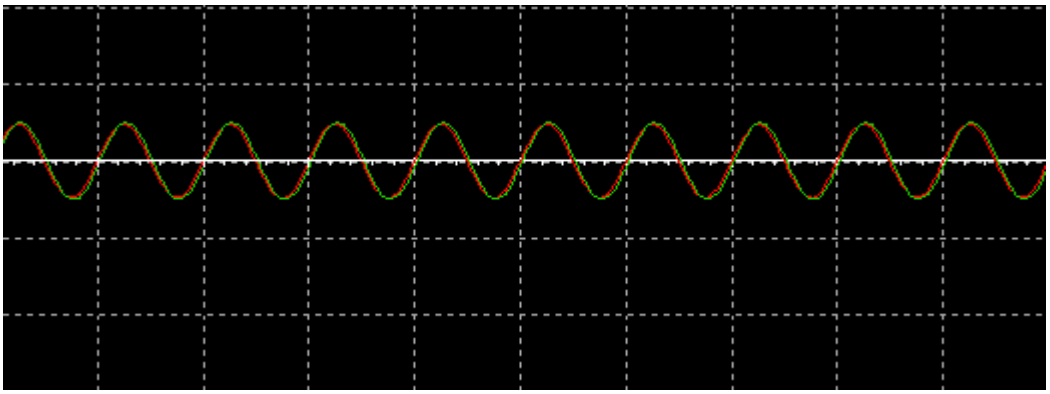
OBSERVATIONS:

From CRO:

1. Input voltage V_i =
2. Output voltage V_0 =
3. Voltage gain $A_V = V_0/V_i$ =

S.NO	**Frequency(Hz)**	**Vo(volts)**	**Gain Av = Vo/V_{in}**	**Gain in dB = 20logAv**

INPUT AND OUTPUT WAVEFORM:



Result:

EXP-8 Date:

Analyze the necessary parameters for NMOS Differential Pair

Aim: Analysis and Verification of Basic NMOS Differential Pair for Gain, Input Common Mode Range, Maximum Input differential voltage requirements

Apparatus: 2N7000 – 2Nos. 100Ω – 2No.s, milliammeter, Function generator, RPS

Procedure:

For all calculations, use the MOSFET parameters given in Table

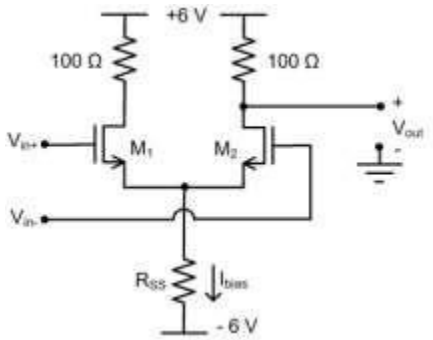
Parameter	Value
V_t	2.1 V
$\mu_n C_{ox}(W/L)$	180 mA/V^2
V_A	50 V

1. For the differential pair shown in Figure, assume that Vin+ = Vin− = 0 V and calculate VGS1 = V_{GS2} for Ibias = 80 mA (remember that I_{bias} will split equally between M1 and M2).
2. Using the value of VGS calculated above, find the value of RSS required to obtain Ibias = 80 mA
3. Calculate the value of VDS for M1 and M2.
4. Assuming a single-ended output (as shown in Fig. 1), calculate the common mode gain (Acm) & differential mode gain for the differential pair using the formulae below

   $A_{CM}=V_2-V_1 / V_{in}$

   $A_{dm=} V_2-V_1 / V_{in}$

   $CMRR = 20*\log_{10}(A_{dm}/ A_{Cm})$



S.No	V_{in}	V_{out}	A_{dm}	A_{cm}	CMRR

EXP-9 Date:

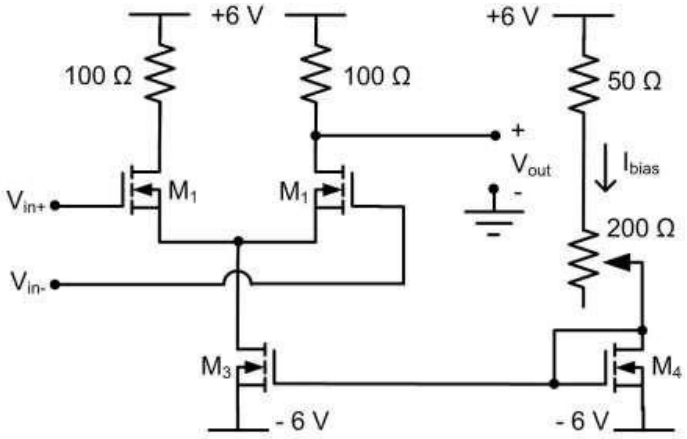
Differential Amplifier with Active Current Mirror Load

Design and Simulation of Differential Amplifier with active current mirror load for gain, powerdissipation & CMRR requirements.

Aim: To measure the differential mode gain, you will need two equal amplitude signals which are opposite in sign using the below circuit obtain a CMRR of 50dB(min).

Apparatus: 2N7000 – 4Nos., Resistor 100 Ω – 2Nos., 50 Ω -1Nos. 200 Ω – 1Nos., multi meter, ammeter and RPS

Circuit Diagram:



Procedure:

For all calculations, use the MOSFET parameters given in Table

Parameter	Value
V_t	2.1 V
$\mu_n C_{ox}(W/L)$	180 mA/V^2
V_A	50 V

1. For the differential pair shown in Figure, assume that Vin+ = Vin− = 0 V and calculate VGS1 = VGS2 for Ibias = 80 mA (remember that I_{bias} will split equally between M1 and M2).
2. Using the value of VGS calculated above, find the value of RSS required to obtain I_{bias} = 80 mA
3. Calculate the value of VDS for M1 and M2.
4. Assuming a single-ended output (as shown in Fig. 1), calculate the common mode gain (Acm) & differential mode gain for the differential pair using the formulae below

$A_{CM}=V_2-V_1 / V_{in}$ Power dissipation = $V_D * I_D$ ($V_D=V_{out}$)

$A_{dm=}$ V_2-V_1 / V_{in}

CMRR = $20*\log_{10}(A_{dm}/ A_{Cm})$

S.No	**V_{in}**	**V_{out}**	**A_{dm}**	**A_{cm}**	**CMRR**

Observations:

Precautions:

1. Do not switch on the power supply until circuit is verified
2. Avoid loose connections on bread board.
3. Handle the apparatus with carefully

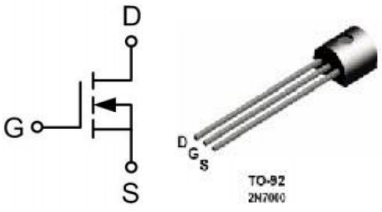
Result:

EXP- 10 Date:

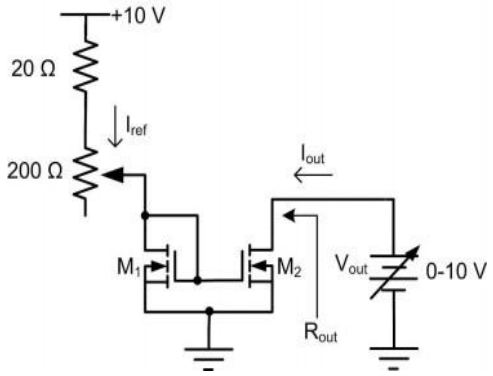
Analyze the basic NMOS current mirror, andcurrent steering circuit

10A) NMOS current mirror

Aim: For the given NMOS parameters design a current mirror circuit using the Iref values as I_{ref} =70mA, 80mA & 90 mA measure the I_{out} current values



Parameter	Value
V_t	2.1 V
$\mu_n C_{ox}(W/L)$	180 mA/V^2
V_A	50 V



Apparatus:

NMOSFET – 2N7000 – 2Nos., potentiometer – 200 Ω, resistor - 20 Ω, multi-meter, milli Ammeter.

Procedure:

Build the circuit shown in figure. The 200 Ω resistor is a potentiometer and the voltage source on the output is a variable DC source. Current measurements can be taken using the readout on the digital power supply, it is not necessary to use the multi-meter. Identify the terminals for each transistor carefully.

1. Adjust the potentiometer until Iref = 80 mA, then measure and record V_{GS1} (the gate-source voltage of M1).
2. Power off the circuit, remove the potentiometer and measure the resistance using the multimeter. Record the total resistance (the measured potentiometer resistance plus the fixed 20 Ω resistor).
3. Replace the potentiometer, power the circuit back on, and adjust the potentiometer until Iref = 70 mA. Measure and record V_{GS1} (the gate-source voltage of M1).
4. Repeat the previous step for Iref = 90 mA

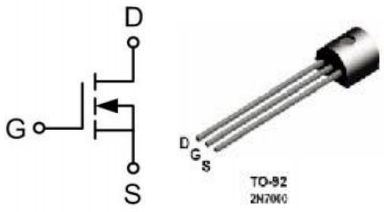
5. Adjust the potentiometer so that Iref = 80 mA again, and measure and record Iout while varying Vout from 0 to 10 volts in 500 mV increments.

6. Set Vout to the measured value of V_{GS} (this gives both transistors the same bias conditions), and measure and record Iout.

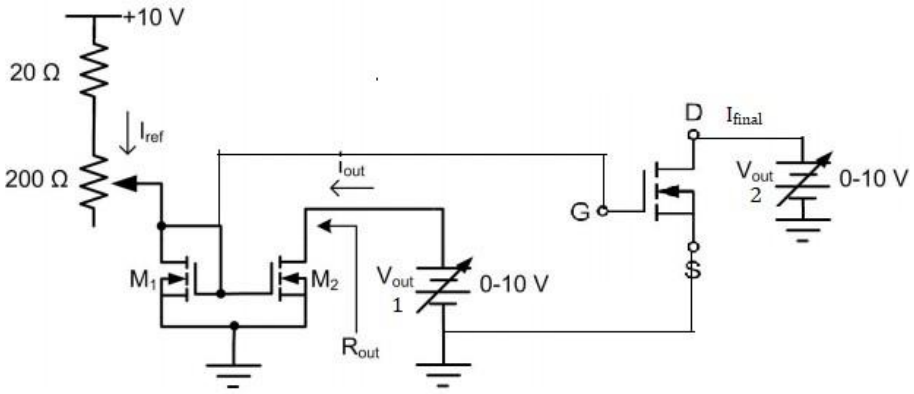
S.No	Iref=70mA			Iref=80mA		
	Applied voltage (V_{out})	V_{GS} (V)	I_{Out} (mA)	Applied voltage (V_{out})	V_{GS} (V)	I_{Out} (mA)

10.B) NMOS CURRENT STEERING CIRCUIT

Aim: : For the given NMOS parameters design a current steering circuit using the Iref values as I_{ref}=20mA to measure the I_{out} & I_{final} current values



Parameter	Value
V_t	2.1 V
$\mu_n C_{ox}(W/L)$	180 mA/V^2
V_A	50 V



APPARATUS:

NMOSFET – 2N7000 – 2Nos., potentiometer – 200 Ω, resistor - 20 Ω, multi-meter, milli Ammeter.

PROCEDURE:

Build the circuit shown in figure. The 200 Ω resistor is a potentiometer and the voltage source on the output is a variable DC source. Current measurements can be taken using the readout on the digital power supply, it is not necessary to use the multi-meter. Identify the terminals for each transistor carefully.

1. Adjust the potentiometer until Iref = 20 mA, then measure and record VGS1 (the gate-source voltage of M1).
2. Power off the circuit, remove the potentiometer and measure the resistance using the multimeter. Record the total resistance (the measured potentiometer resistance plus the fixed 20 Ω resistor).
3. Replace the potentiometer, power the circuit back on, and adjust the potentiometer until Iref = 70 mA. Measure and record VGS1 (the gate-source voltage of M1).
4. Repeat the previous step for Iref = 90 mA
5. Adjust the potentiometer so that Iref = 20 mA again, and measure and record Iout & I_{final} while varying V_{out1} & V_{out2} from 0 to 10 volts in 500 mV increments.

S.No	Iref=20mA				
	Applied voltage (V_{out})	V_{GS1} (V)	I_{Out1} (mA)	V_{GS2} (V)	I_{final} (mA)

EXP-11 Date:

SIMULATION AND PCB FABRICATION OF A BJT MULTIVIBRATOR CIRCUIT

Aim:

To design an astable Multivibrators circuit, to produce a series of pulses at a frequency of nearly 70kHz with a mark-to-space ratio of 1:5. If R2 = R3 = 1kΩ, Calculate the values of the capacitors, C1 and C2 required. Simulate and fabricate a PCB with the designed values.

Apparatus:

H/W : Transistors – BC 107 – 2No.s
Resistors – 1KΩ / 2.2 kΩ / 10 kΩ each - 4No.s
Capacitors – 0.1 µF, 0.01µF
RPS, CRO, Probes, Bread board, connecting wires
PCB-1No. Etching solution, Ironing,
S/W : Personal computer, Multisim software, PCB123

Theory:

Astable Multivibrators are the most used type of relaxation oscillator because not only are they simple, reliable and ease of construction they also produce a constant square wave output waveform.

Astable multivibrators are also known as Free-running Multivibrator as they do not require any additional inputs or external assistance to oscillate. Astable oscillators produce a continuous square wave from its output or outputs, (two outputs no inputs) which can then be used to flashlights or produce a sound in a loudspeaker.

The basic transistor circuit for an Astable Multivibrator produces a square wave output from a pair of grounded emitter cross-coupled transistors. Both transistors either NPN or PNP, in the multivibrator are biased for linear operation and are operated as Common Emitter Amplifiers with 100% positive feedback.

Basic Astable Multivibrator Circuit

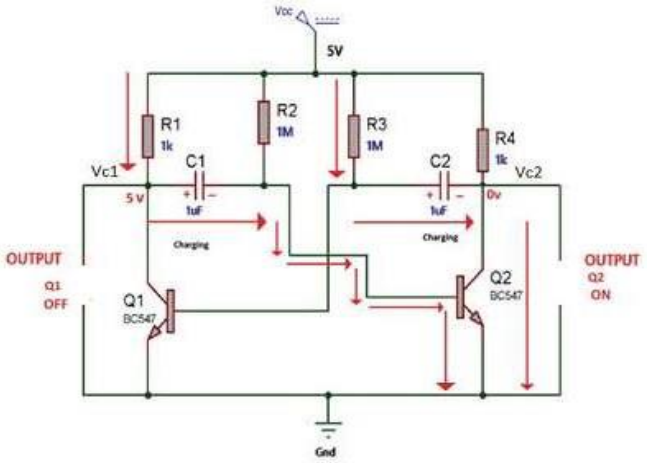


Figure 11 Transistor Astable multivibrator

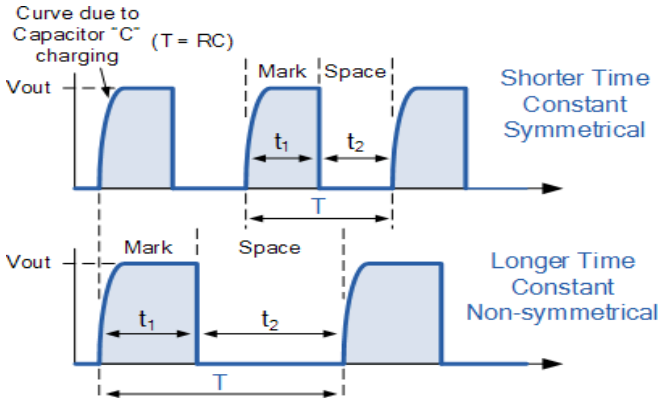


Figure11(b) Output Waveforms

Unlike the Monostable Multivibrator or the Bistable Multivibrator, the Astable Multivibrator has automatic built in triggering which switches it continuously between its two unstable states both set and reset.

Hints: Formulae required for calculation:

For frequency calculation use

$F=1/T = 1/ (1.38* R*C)$

Periodic Time $T= t_1+t_2$

$t_1=0.69*C_1*R_3$ $t_2 =0.69*C_2*R_2$

Where, R is in Ω's, C is in Farads, T is in seconds and *f* is in Hertz.

and by rearranging the formula above for the periodic time, the values of the capacitors required to give a mark-to-space ratio of 1:5 are to be calculated

Procedure:

1. Connect the circuit as per the circuit diagram.
2. Apply biasing voltage to the circuit by using RPS (0-15V)
3. Connect the CRO probes at the outputs as indicated in the circuits
4. Measure the CRO wave form time periods and voltages for plotting graphs
5. Compare the time periods with the theoretical values.
6. Repeat the above procedure for different frequencies by varying the resistor or capacitor values (R2,R3 or C1,C2)

Precautions:

4. Do not switch on the power supply until circuit is verified
5. Avoid loose connections on bread board.
6. Handle the apparatus with carefully

Result:

PCB Fabrication:

A PCB layout created by the designer using PCB design software. Commonly used PCB design software includes PCB123, Altium Designer, OrCAD, Pads, KiCad, Eagle etc

The etching process can be carried out in several ways. The most commonly used method for etching is by using hydrochloric acid or ferric chloride. Both the chemicals are plentiful and economical. The main purpose of the PCB etching process is to trace the circuit design on a copper plate. To do this, there are several steps that you need to follow, which are as follows:

Step 1: The very first step of the etching process is designing the circuit, using the software of your choice. Once the design is ready, flip it, and then get it printed.

Step 2:On the transfer paper, print the circuit design. Make sure that the design is printed on the shiny side of the paper.

Step 3: Now, take the copper plate, and rub sandpaper on it. This will make the surface of copper rough, and thus helps it to hold the design efficiently. There are certain points to remember step 3 till the last step:

- Use safety gloves, while handling copper plate and etching solution. This will prevent the oil from hands getting transferred to copper plate and will also protect your hands from the solution or chemicals.
- When we are sanding the copper plate, make sure you do it properly especially at the edges of the plate.

Step 4: Now, wash the plate by some rubbing alcohol and water, so that any small particles of copper that get removed from the surface during sanding are washed off. Allow the plate to dry after washing.

Step 5: Cut the printed design properly and place them on the copper plate facing down.

Step 6: The copper plate is now passed through the laminator several times until the plate gets heated.

Step 7: Take the plate out from the laminator, after it is hot, and hold it in a cold bath. Agitate the plate so that all the paper comes off and floats on the water. You will see a traced circuit in black on the copper plate.

Step 8: Now take the board out of the bath, and place it in the etching solution. Agitate the copper plate for around 30 minutes. Ensure that all the copper around the design is dissolved.

Step 9: Take out the copper plate and wash it in the water bath again. Keep it to dry. Once it has dried completely, you can use rubbing alcohol to remove the ink transferred to the printed circuit board.

Step 10: This completes the etching process of a printed circuit board. You can now drill the holes using proper tools with the required drill bit size.

Reference : Table for Capacitor Vs Resistance for various frequencies

Res.	Capacitor Values								
	1nF	2.2nF	4.7nF	10nF	22nF	47nF	100nF	220nF	470nF
1.0kΩ	714.3kHz	324.6kHz	151.9kHz	71.4kHz	32.5kHz	15.2kHz	7.1kHz	3.2kHz	1.5kHz
2.2kΩ	324.7kHz	147.6kHz	69.1kHz	32.5kHz	14.7kHz	6.9kHz	3.2kHz	1.5kHz	691Hz
4.7kΩ	151.9kHz	69.1kHz	32.3kHz	15.2kHz	6.9kHz	3.2kHz	1.5kHz	691Hz	323Hz
10kΩ	71.4kHz	32.5kHz	15.2kHz	7.1kHz	3.2kHz	1.5kHz	714Hz	325Hz	152Hz
22kΩ	32.5kHz	14.7kHz	6.9kHz	3.2kHz	1.5kHz	691Hz	325Hz	147Hz	69.1Hz
47kΩ	15.2kHz	6.9kHz	3.2kHz	1.5kHz	691Hz	323Hz	152Hz	69.1Hz	32.5Hz
100kΩ	7.1kHz	3.2kHz	1.5kHz	714Hz	325Hz	152Hz	71.4Hz	32.5Hz	15.2Hz
220kΩ	3.2kHz	1.5kHz	691Hz	325Hz	147Hz	69.1Hz	32.5Hz	15.2Hz	6.9Hz
470kΩ	1.5kHz	691Hz	323Hz	152Hz	69.1Hz	32.5Hz	15.2Hz	6.6Hz	3.2Hz
1MΩ	714Hz	325Hz	152Hz	71.4Hz	32.5Hz	15.2Hz	6.9Hz	3.2Hz	1.5Hz